北京大学
PEKING UNIVERSITY

智能硬件体系结构

第二讲Supp：电路基础-晶体管与数字电路设计

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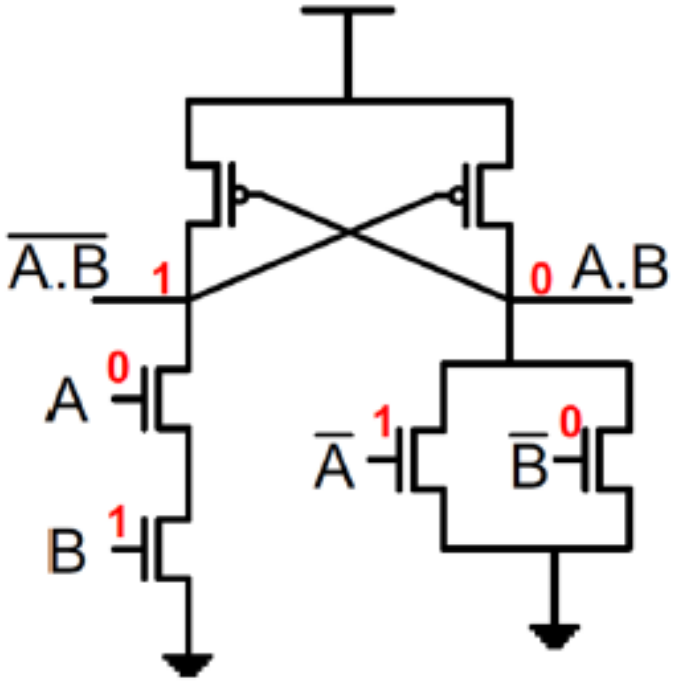
DCVS静态逻辑电路

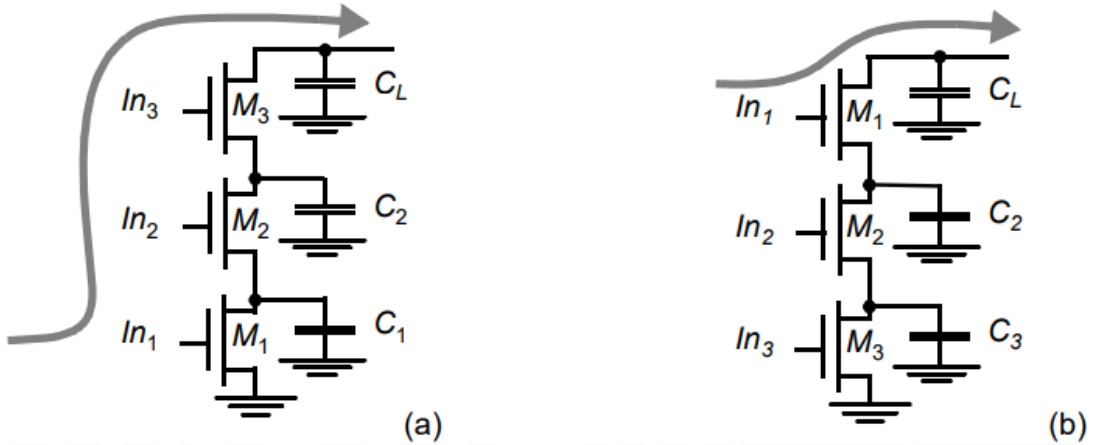
- 关于NAND电路中PUN上拉能力



- 左边pMOS与右边pMOS构成锁存结构
- **最坏情况下**
  - ①左边上拉能力比两个nMOS串联下拉能力弱
  - ②右边需要比一个nMOS下拉能力弱
- 对于①：$\overline{AB}$ 在需要被下拉时A与B均为1，因此nMOS、pMOS需要同时打开，因此只有pMOS上拉能力较弱才能迅速完成对输出节点$\overline{AB}$的下拉
- 对于②：AB在需要下拉时$\overline{AB}$为0，因此同理也是一个pMOS上拉与一个nMOS下拉对抗（worst case）

Transistor Ordering (Input Re-Ordering) , P29

- 通过重新排列input和transistor位置来得到更小的delay



- **不同input对于output的delay是不同的**，如上图(a)中In1比其余两个输入对输出延迟更大（In1引起的跳变需要3个电容均放电，In3仅C_L会发生放电），因此**In1为这个设计下的critical path**
- 然而不同信号到达当前这个门的delay时间也不同，可能In1本身就是最晚到达的，此时假设按(b)那样设计，整体看**critical path仍然是In1**（因为In1到达时间最晚），然而**总延迟被缩小**（因为在图中这个逻辑门中延迟减小了）

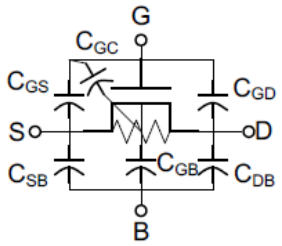
参考Digital Integrated Circuits - A Design Perspective P243

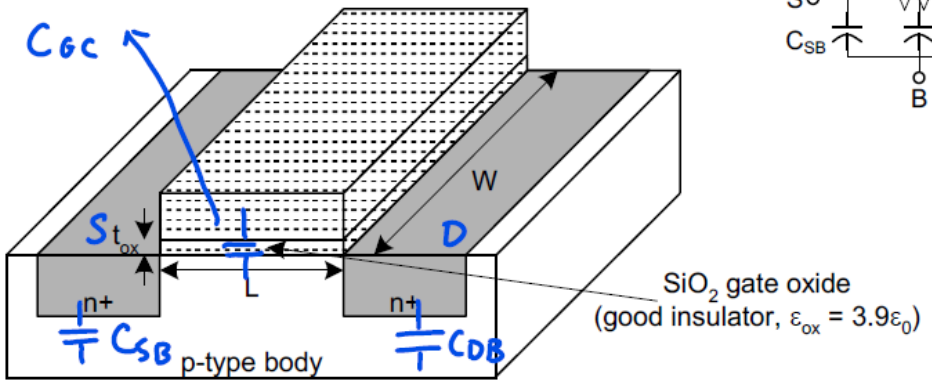
延迟计算（PPT P33）

- MOS寄生电容

Gate Capacitance

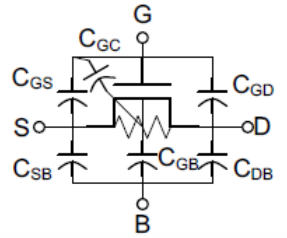
- Gate capacitance can be complex, but we will use a simple model
- $C_{GC} = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL = C_{per\_micron}W$
- C_{per_micron} about 1.3fF/μm

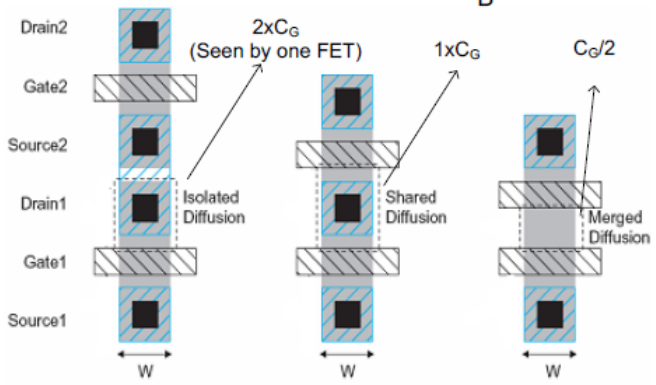




Diffusion Capacitance

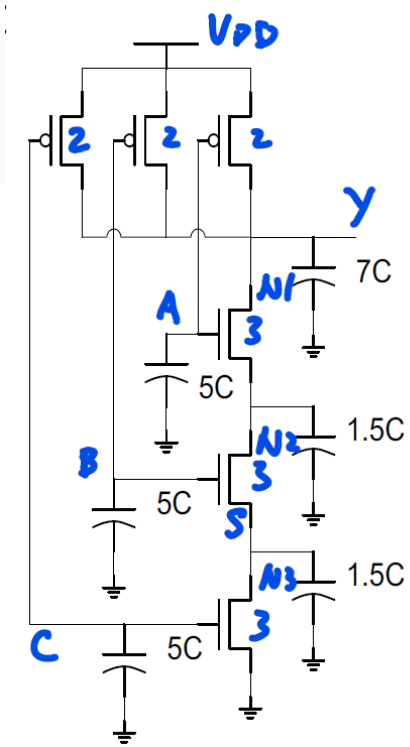
- C_{SB}, C_{DB}
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to C_G for contacted diff
  - ½ C_G for uncontacted
  - Varies with process

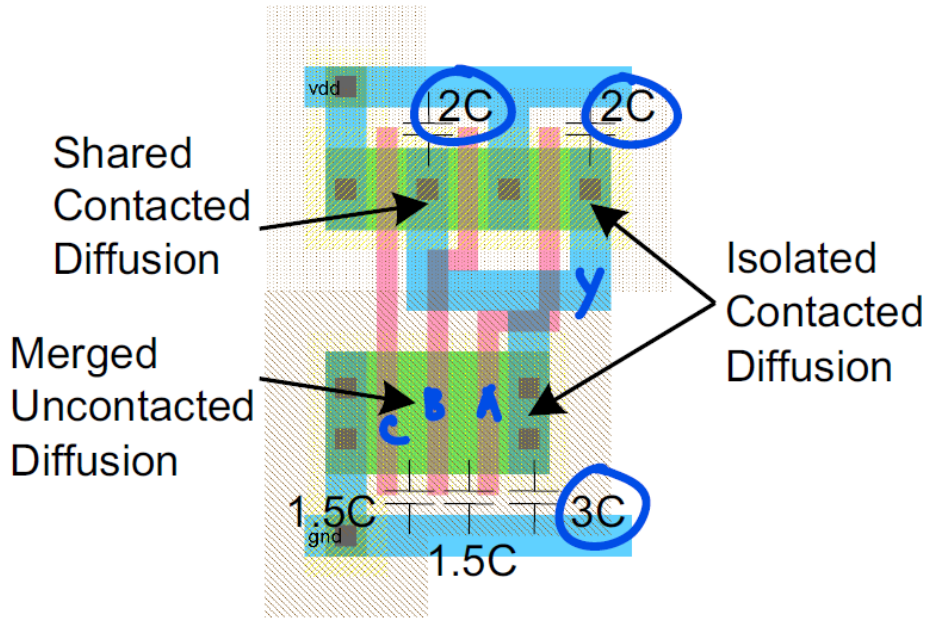




延迟计算（PPT P33）

- NAND Gate版图



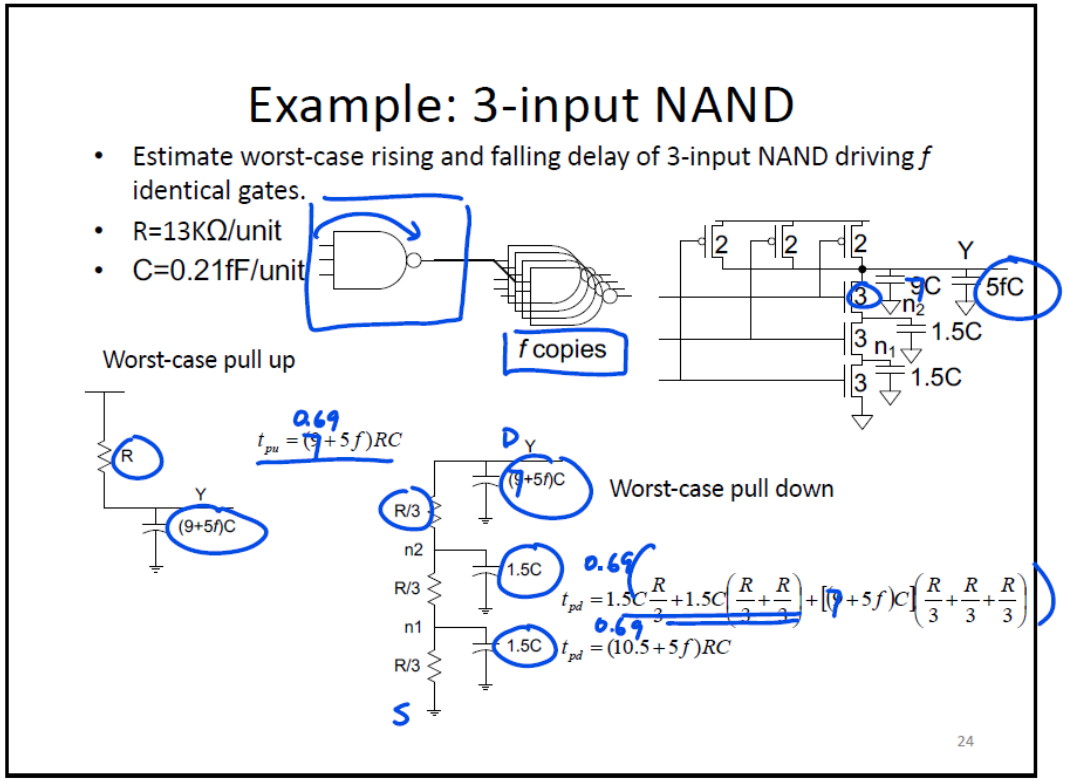


对于输出节点Y，寄生电容为

$$2C + 2C + 3C = 7C$$

延迟计算（PPT P33）

- 3-input NAND pull down delay



以后作业考试中类似题目都将直接标出寄生电容

- 笔记中标注的是正确条件
- $t_{pd} = 0.69 \times [1.5C \times \frac{R}{3} + 1.5C\left(\frac{R}{3} + \frac{R}{3}\right) + (7 + 5f)C \times \left(\frac{R}{3} + \frac{R}{3} + \frac{R}{3}\right)] = (5.87 + 3.45f)C$

利用logical effort进行延迟计算（P42 P43）

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- **Logical Effort定义**

- Express delays in process-independent unit $d = \frac{d_{abs}}{\tau}$
- Delay has two components: d = f + p
- *f*: *effort delay* = *gh* (a.k.a. stage effort)
  - Again has two components
- *g*: *logical effort*
  - Measures relative ability of gate to deliver current
  - *g* =1 for inverter
- *h*: *electrical effort* = C_{out} / C_{in}
  - Ratio of output to input capacitance
  - Sometimes called fanout
- *p*: parasitic delay
  - Represents delay of gate driving no load
  - Set by internal parasitic capacitance

τ = 3RC
≈ 3 ps in 65 nm process
60 ps in 0.6 μm process

参考补充材料Logical Effort - 1

- 排除工艺节点的影响
- 以INV的标准延迟作为一个单位
- Delay分为两个部分
  - 一部分由drive外部负载能力组成（f)
  - 一部分由逻辑门内部自身transition delay构成 (p)

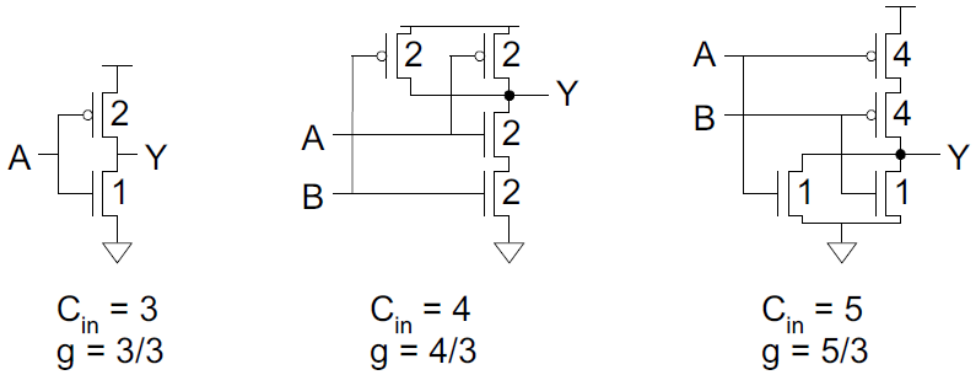
f = g · h

g: 由逻辑门deliver电流能力决定
h: 由负载大小决定

利用logical effort进行延迟计算（P42 P43）

- 逻辑门的g值

- DEF: *Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current*.
- Measure from delay vs. fanout plots
- Or estimate by counting transistor widths



C_{in} = 3
g = 3/3

C_{in} = 4
g = 4/3

C_{in} = 5
g = 5/3

按照worst case进行计算，比如图中间的NAND的上拉部分应该按照一个管子导通时deliver电流的能力和INV相同，因此这里的一个pMOS宽度为2个单位而非4个单位，因此总输入电容为4个单位

参考补充材料Logical Effort - 1

利用logical effort进行延迟计算（P42 P43）

- 多级级联的Path Delay计算

  - Path Effort Delay $D_F = \sum f_i$
  - Path Parasitic Delay $P = \sum p_i$
  - Path Delay $D = \sum d_i = D_F + P$
  - Delay is smallest when each stage bears same effort

    $\hat{f} = g_i h_i = F^{\frac{1}{N}}$
  - Thus minimum delay of N stage path is

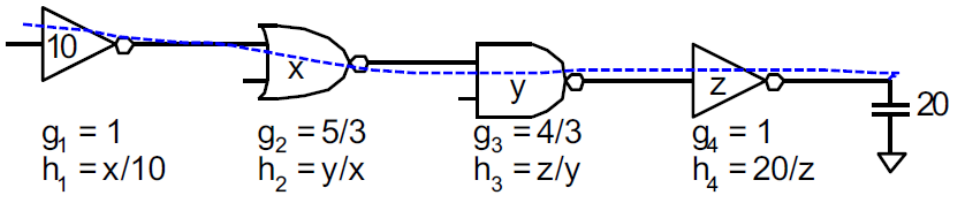
    $D = NF^{\frac{1}{N}} + P$
  - This is a key result of logical effort
    - Find fastest possible delay
    - Doesn't require calculating gate sizes

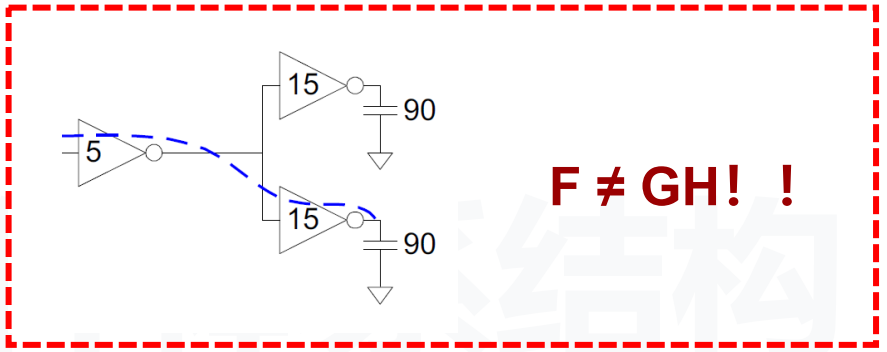
参考补充材料Logical Effort - 1

利用logical effort进行延迟计算（P42 P43）

- 多级级联的Path Effort Delay计算

  - Logical effort generalizes to multistage networks
  - *Path Logical Effort* $G = \prod g_i$
  - *Path Electrical Effort* $H = \dfrac{C_{\text{out-path}}}{C_{\text{in-path}}}$
  - *Path Effort* $F = \prod f_i = \prod g_i h_i$





  - Introduce *branching effort*
    - Accounts for branching between stages in path

$$b = \frac{C_{\text{on path}} + C_{\text{off path}}}{C_{\text{on path}}}$$

$$B = \prod b_i$$

Note:

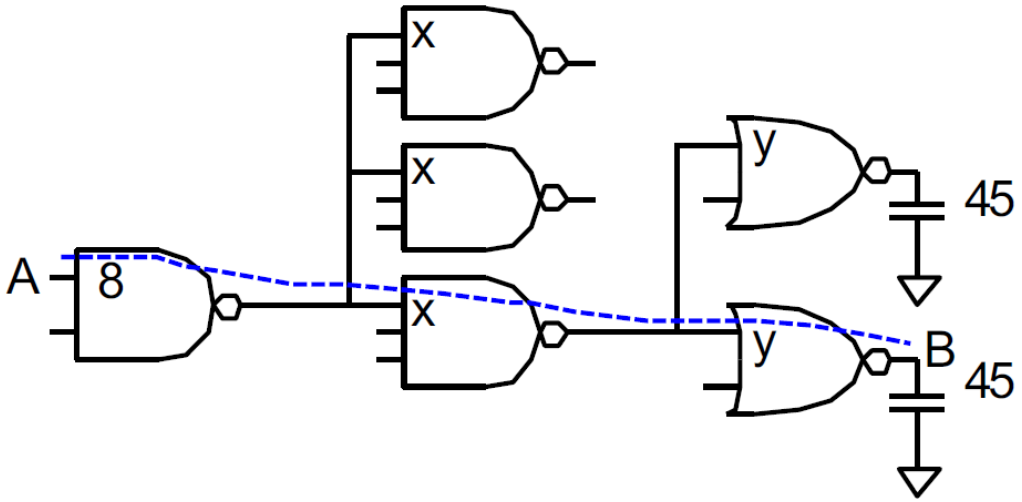
$$\prod h_i = BH$$

  - Now we compute the path effort
    - F = GBH

参考补充材料Logical Effort - 1

利用logical effort进行延迟计算（P42 P43）

- 举例：设计x y使A到B的Path Delay最小



$$BH = \frac{3x}{8}\frac{2y}{x}\frac{45}{y} = \frac{135}{4}$$

$$G = \frac{4}{3} \times \frac{5}{3} \times \frac{5}{3} = \frac{100}{27}$$

$$F = GBH = 125$$

delay最小时**各级effort相同**

$$f = \sqrt[3]{F} = 5$$

故有下列三个等式

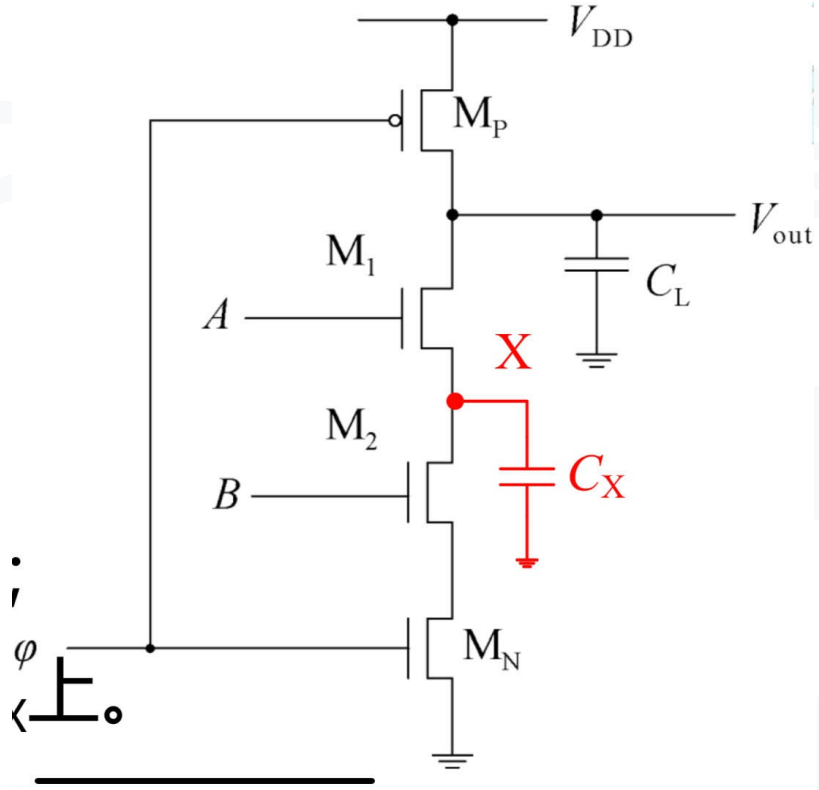
$$5 = \frac{4}{3} \times \frac{3x}{8} \quad , \quad 5 = \frac{5}{3} \times \frac{2y}{x} \quad , \quad 5 = \frac{5}{3} \times \frac{45}{y}$$

可得x=10, y=15

参考补充材料Logical Effort - 1

动态电路存在的问题(P47)

- **电荷分享问题**



- X点存在寄生电容C_X
- 预充阶段，A=B=0，C_L被充电，C_X未被充电
- 求值阶段，A=1，B=0，M_1将C_L电荷传输到C_X上

由电荷守恒得

$$Q_{sum} = C_L V_{DD} = (C_X + C_L)V_f$$

假设达到平衡时，V_{OUT}与V_X相等均为V_f，则

$$V_{OUT} = V_f = \frac{V_{DD}}{1 + \frac{C_X}{C_L}}$$

假设达到平衡时，$V_X = V_{DD} - V_{TN}$，M_1截止，则

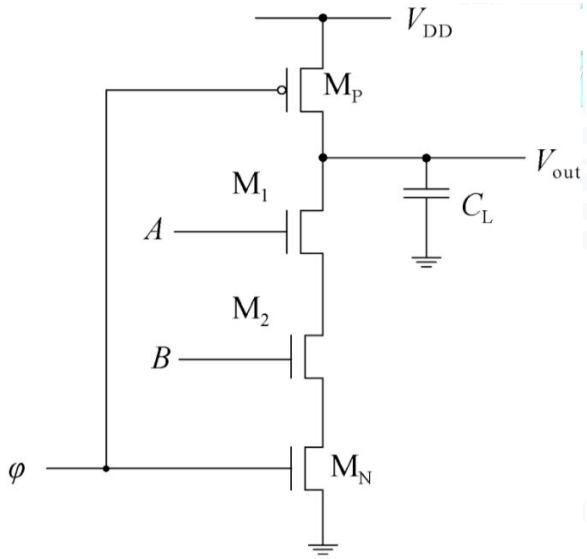
$$V_{OUT} = V_f = V_{DD} - \frac{C_X}{C_L}(V_{DD} - V_T)$$

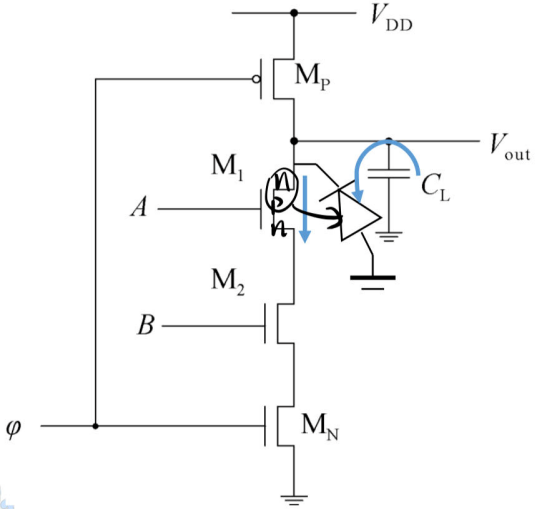
非理想V_{DD}

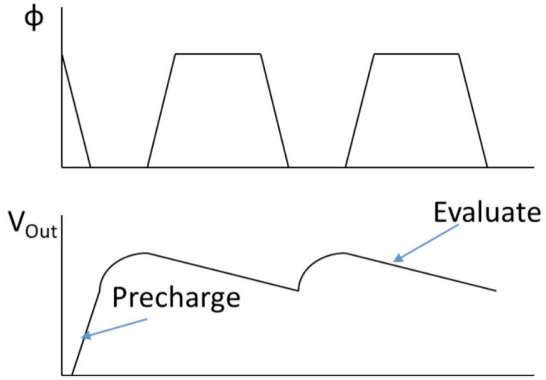
参考王源老师集成电路设计原理PPT

动态电路存在的问题(P47)

- 电荷泄露问题







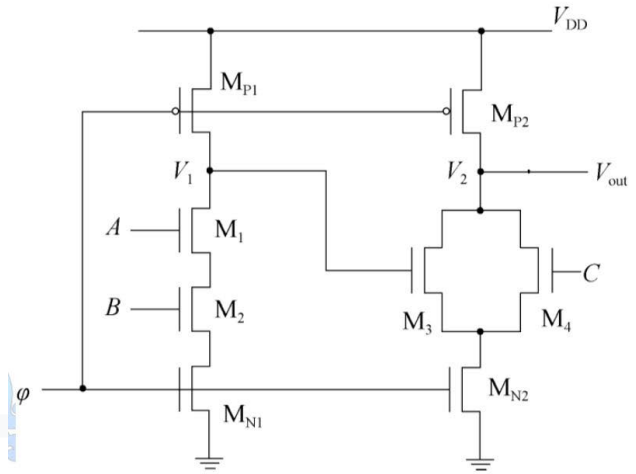
M1为nMOS，结构为npn，因此源端与体端为np构成一个**反偏的二极管，**

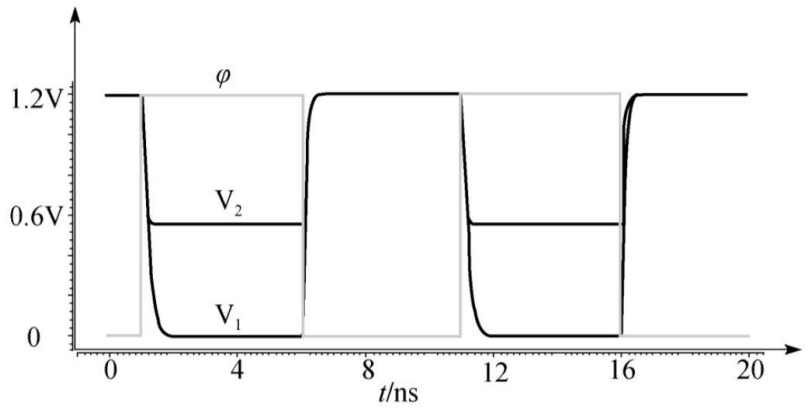
该二极管有持续的反偏电流漏电导致动态电路无法长时间保持状态不变

参考王源老师集成电路设计原理PPT

动态电路存在的问题(P47)

- 级联问题（为什么Domino电路级联要加级间反相器）
  - 在预充阶段，V_1为高电平，导致M3被打开
  - 当φ拉高时，M3不能及时关闭，导致V2节点电压被下拉，可能导致后面一级出现逻辑错误
  - 因此Domino级间使用INV连接，在预充时保证不会将下一级的晶体管打开





参考王源老师集成电路设计原理PPT