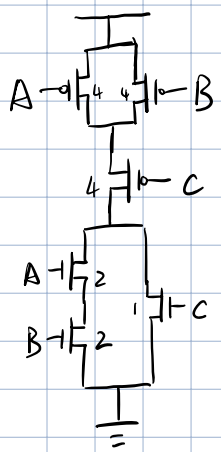
1. 1) $OUT = A \cdot SEL + B \cdot \overline{SEL}$

$= \overline{\overline{A \cdot SEL} \cdot \overline{(B \cdot \overline{SEL})}}$

$\Rightarrow$ 4个 NAND 实现

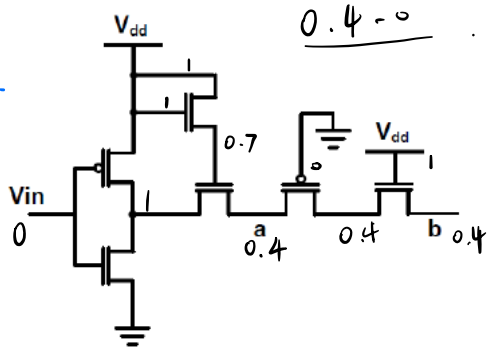
2) $OUT = \overline{AB+C}$

对于C的 logical effort 为 $g = 5/3$



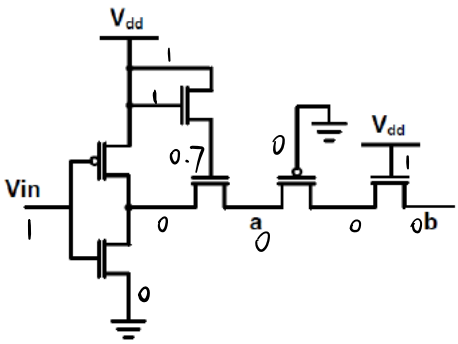
3) (1)

本题假设初态 $V_a = V_b = 0$

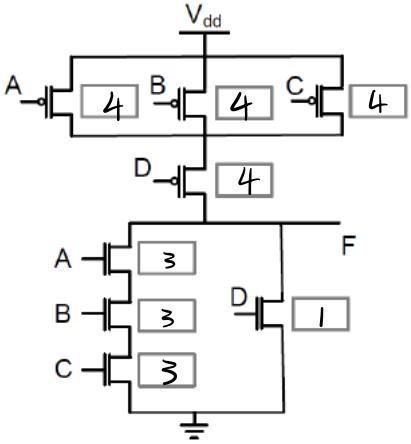


0.4 - 0

(2)



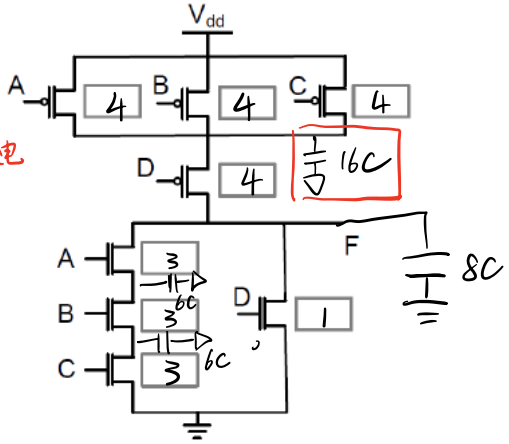
4)



$F = \overline{ABC+D}$

5)

不考虑 PMOS 处电容放电



A: $t_A = \ln 2 \cdot 8C \cdot (\frac{R}{3} \cdot 3) = 8\ln 2\, RC$

B: $t_B = \ln 2 \cdot (\frac{2R}{3} \cdot 6C + 8C \cdot R) = 12\ln 2\, RC$

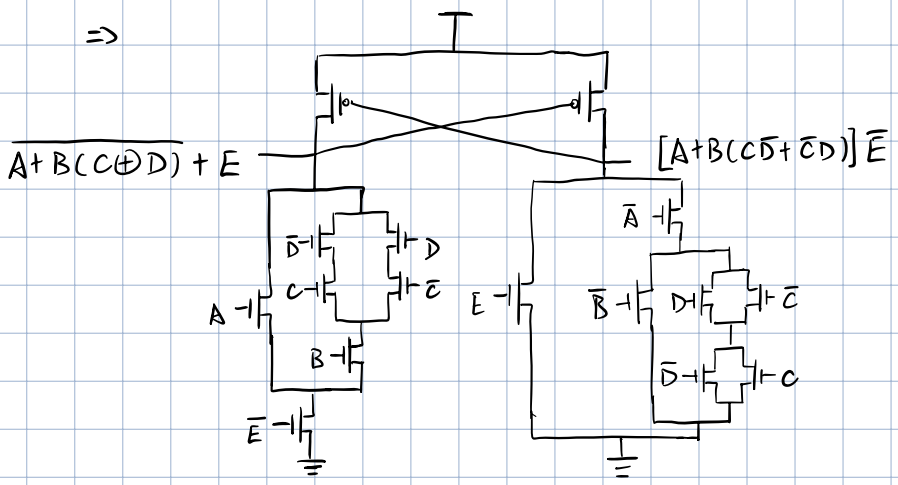
C: $t_C = \ln 2 \cdot [\frac{R}{3} 6C + 6C(\frac{R}{3} + \frac{R}{3}) + 8C \cdot R] = 14\ln 2 \cdot RC$

D: $t_D = \ln 2 \cdot 8C \cdot R = 8\ln 2\, RC$

6) $\overline{A+B(C\oplus D)}+E = \overline{[A+B(C\oplus D)]\bar{E}}$

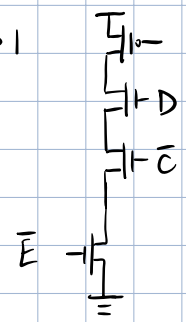
$= \overline{[A+B(C\bar{D}+\bar{C}D)]\bar{E}}$

=>



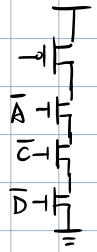
D导致的翻转.

输出 0=>1



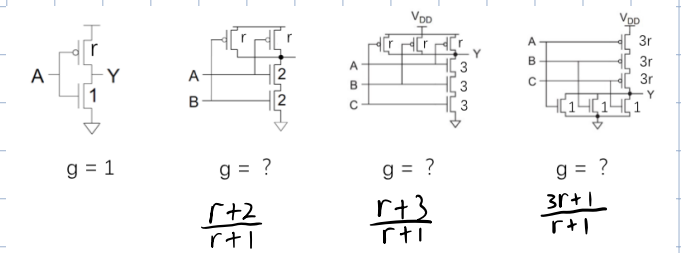
三个nMOS串联下拉能力大于1个pMOS上拉能力

输出 1=>0



同理，三个nMOS串联下拉能力大于1个pMOS上拉能力

2. 1a)



1b) $G = \Pi g_i = \frac{4r+1}{r+1} \cdot 1 \cdot \frac{r+2}{r+1} = \frac{65}{16}$

$H = \frac{C_{out}}{C_{in}} = 8$

$B = \Pi b_i = 3 \times 4 = 12$

故 $F = GBH = 390$

$f = \sqrt[3]{F} = 7.31$

每一级 Logical Delay 相同时总 Delay 最小

得 $C_x = 3.75C$, $C_y = 6.84C$

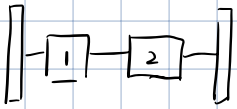
$D = F + P = 3 \cdot f + \sum P_i = 3 \times 7.31 + (\frac{4r+4}{r+1} + 1 + \frac{2r+2}{r+1}) = 28.93$

2a) 若工作在 800MHz，则 Circuit 1/2 的延迟之和需要小于时钟周期（最大延迟）

$T \geq t_{c\to q} + t_1 + t_2 + t_{setup}$

$1.25\,ns \geq 0.35\,ns + \frac{1.0}{N} + 0.6 + 0.15\,ns$

$N \geq 6.67$



至少 6.67 倍

Hold constraint check: $t_{hold} \leq t_{1,min} + t_{2min} + t_{c\to q,min}$ 满足要求

2b) 最快时钟下需要保证 setup 与 hold 条件能够满足

$$\begin{cases} T \geq t_{c\to q,max} + t_{1,max} + t_{2,max} + t_{setup} \\ t_{hold} \leq t_{c\to q,min} + t_{1,min} + t_{2,min} \end{cases}$$

又有 $t_{1,max} + t_{2,max} = 2(t_{1min} + t_{2,min})$

故 $T - t_{c\to q,max} - t_{setup} \geq 2(t_{hold} - t_{c\to q,min})$

得 $T \geq 0.7\,ns$

最大频率为 $f_{max} = \frac{1}{T_{min}} = 1.43\,GHz$

3) 为保证输出结果正确，寄存器级间需满足 setup 与 hold 条件

$$\begin{cases} T \geq t_{c\to q} + t_{logic} + t_{setup} + \delta_{min} \\ t_{hold} \leq t_{c\to q} + t_{logic} - \delta_{max} \end{cases}$$ → skew 总会使得系统更坏

有 $\begin{cases} T \geq 150ps + \frac{100ns}{N} + 100ps + 70ps \times N^2 \\ 60p \leq 150ps + \frac{100ns}{N} - 70ps \times N^2 \end{cases}$

解得 $\begin{cases} N \leq 11.3 \\ T \geq 250ps + \frac{100ns}{N} + 70ps \times N^2 \end{cases}$

当 N 取 9 时，T 最小为 17.03 ns

频率最大为 58.7 MHz

4a) logical effort delay 为 $F = \sum g \cdot h = \frac{C_{in2}+50fF}{5fF} + \frac{80fF+C_{in3}}{C_{in2}} + \frac{500fF}{C_{in3}}$

优化目标为使 F 最小，有解得 $\begin{cases} C_{in2} = 32.15\,fF \\ C_{in3} = 126.8\,fF \end{cases}$ ← 解 $\begin{cases} \frac{\partial F}{\partial C_{in2}} = 0 \\ \frac{\partial F}{\partial C_{in3}} = 0 \end{cases}$

得最小的延迟为 $t_{delay} = (F+P)t_{p0} = 596\,ps$

4b) 取 C_{in2} 为 30 fF，C_{in3} 为 130 fF，算得

$t_{delay} = (F'+P)t_{p0} = 597\,ps$

3、1) 状态机逻辑为（@ posedge CLK）

```
if (X=0) begin
    if B    X<=0
    if !B   X<=1
end
else if (X=1) begin
    if (AB)  X<=1
    if !(AB)  X<=0
```

故使用一个寄存器来存储 X，其输入有

$IN = (!X)(!B) + (X)(AB)$

=> 由此可得电路图如右图所示